High Performance Low Power Consumption Differential Input Single-ended Output CMOS OpAmp

SME307 Report, a design of two stage operational amplifier with specifications

FENG Shuo
Southern University of Science and Technology
School of Microelectronics
Shenzhen, China
11911736@mail.sustech.edu.cn

WANG Haoyu
Southern University of Science and Technology
School of Microelectronics
Shenzhen, China
11911134@mail.sustech.edu.cn

***Abstract*—This experiment aims to design a differential input single-ended output CMOS Operational amplifier (OpAmp). As for the tool, we use Cadence to design and simulate. We modified the parameters to achieve the requirement. After many efforts, the circuit has a good performance with low power.**

***Index Terms*—analog IC design, CMOS, opamp**

I. Introduction

Based on the knowledge we learnt in the course of Design of Analog CMOS Integrated Circuits, we determined the circuit structure as the two-stage amplifier structure since the single-stage difference pair structure cannot achieve a high gain.

As for the condition, we can use the DC voltage $V_{DD} = 1.8V$ with the load equals to $1pF$. And we use the process of $0.18\mu m$.We modified the parameters many times to accomplish the requirement.

This report shows the process from designing the circuit to modifying the parameters. It also includes the ultimate datas and the simulation results.

II. Circuit Design and Derivation

In this section, we display our design thought of the circuit and the formula derivation of the important parameters. The global circuit is shown in fig 1.

A. Designing the Circuit

As shown in the fig 1, our circuit is mainly composed of four sections classified by functions. The first section is the bias circuit. The second section is the first stage amplification circuit. The third section is the second stage amplification circuit. The forth section is the compensating circuit.

The bias circuit is accomplished by the current mirror. The large size current mirror can also decrease the current deviation caused by channel length modulation and improve the stability of the circuit. There are two current mirrors in the circuit. One is composed of MN5 and MN8, and the other one is composed of MN7 and MN8. It is an active device, we use a current source to provide the bias current.

The first stage amplification circuit is a differential amplification circuit. It is composed of MN1,MN2,MP3 and MP4. Since the differential pair should be symmetric in order to get the best performance, the parameters of W and L should be identical for corresponding transistors. As is shown in the fig 1, MN1 and MN2 are identical NMOS while MP3 and MP4 are identical PMOS. As for the tail transister MN5, it provides bias current for the first stage.

The second stage amplification circuit is a common source structure composed of MP6 and MN7. The bias current is provided by MN7. The input of the second stage is the output of the first stage. And the final output of the whole circuit is the output of the second stage.

The compensating circuit is composed of Rc and Cc, which accomplish the Miller compensation.

In order to have a more clear view of our OpAmp, we have made a symbol in fig 2.

B. Derivation of Formulas

In this part, we will show the derivation of the important parameters, including the voltage gain, poles, slew rate, transconductance, phase margin and unity gain frequency.

- **Frequency Characteristics**
  The equivalent circuit of small signal analysis(ignoring R_c) is shown in fig3.
  The input of the first stage is a differential input. Since MN1 and MN2 are identical transistors, we know

$$G_{m1} = g_{m1} = g_{m2} \tag{2.1}$$

  R_1 represents the output of the first stage. The value of R_1 is

$$R_1 = r_{o2} \| r_{o4} \tag{2.2}$$

  So the voltage gain of the first stage is

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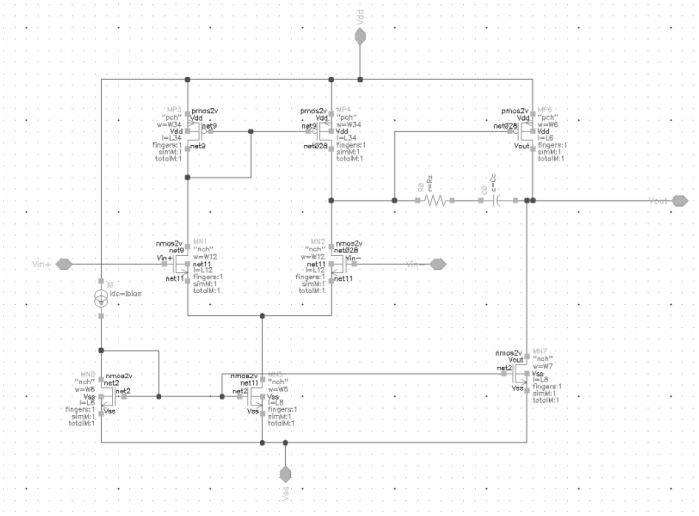

Fig. 1. Schematic Diagram of the Design Cadence Structure

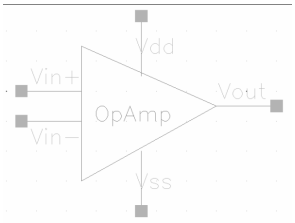

Fig. 2. Symbol of the OpAmp

$$A_1 = G_{m1}R_1 = g_{m2}(r_{o2}\|r_{o4}) \tag{2.3}$$

For the second stage,

$$G_{m2} = g_{m6} = \frac{2I_{DS6}}{V_GST6} \tag{2.4}$$

$$R_2 = r_{o6}\|r_{o7} \tag{2.5}$$

And the voltage gain of the second stage is

$$A_2 = -G_{m2}R_2 = -g_{m6}(r_{o6}\|r_{o7}) \tag{2.6}$$

So the overall DC open-loop voltage gain is

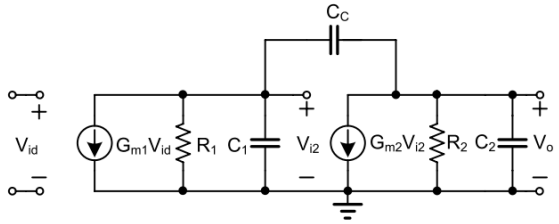

Fig. 3. Small Signal Analysis Equivalent Circuit

$$A_0 = A_1A_2 = -g_{m2}g_{m6}(r_{o2}\|r_{o4})(r_{o6}\|r_{o7}) \tag{2.7}$$

Set $V_{GST} = v_{GS} - V_T$, we can get

$$g_m = \mu C_{ox}\frac{W}{L}(V_{GS} - V_T) = \frac{2I_D}{V_{GST}} \tag{2.8}$$

r_o is decided by

$$r_O = \frac{1}{\lambda I_{DS}} \tag{2.9}$$

C_1 is the capacitance between the first-stage output node and ground.

$$C_1 = C_{GD2} + C_{DB2} + C_{GD4} + C_{DB4} + C_{GS6} \tag{2.10}$$

C_2 is the capacitance between the second-stage output node and ground.

$$C_2 = C_{DB6} + C_{DB7} + C_{GD7} + C_L \tag{2.11}$$

In general, C_L is much larger than the capacitance of transistor, so $C_2 \gg C_1$
According to the Kirchhoff's Current Law, we can get

$$G_{m1}V_{id} + \frac{V_{i2}}{R_1} + sC_1V_{i2} + sC_c(V_{i2} - V_o) = 0 \tag{2.12}$$

$$G_{m2}V_{i2} + \frac{V_o}{R_2} + sC_2V_{i2} + sC_c(V_o - V_{i2}) = 0 \tag{2.13}$$

Connect above two equations, we can get the transfer function of the circuit.

$$\frac{V_o}{V_id} = \frac{G_{m1}(G_{m2} - sC_c)R_1R_2}{as^2 + bs + 1} \tag{2.14}$$

in which

$$a = [C_1C_2 + C_c(C_1 + C_2)R_1R_2] \tag{2.15}$$

and

$$b = C_1R_1 + C_2R_2 + C_c(G_{m2}R_1R_2 + R_1 + R_2) \tag{2.16}$$

We can get the zero point in the right plane according to the numerator of equation (2.14).

$$f_z = \frac{G_{m2}}{2\pi C_c} = \frac{g_{m6}}{2\pi C_c} \tag{2.17}$$

For the equation forming as $as^2 + bs + c = 0$, if two real roots exist, then the roots are $s_1 = -c/b$, $s_2 = -b/a$. According to the denominator of equation (2.14), we get the two real roots.

$$s_1 = -\frac{1}{C_1R_1 + C_2R_2 + C_c(G_{m2}R_1R_2 + R_1 + R_2)} \tag{2.18}$$

$$s_2 = -\frac{C_1R_1 + C_2R_2 + C_c(G_{m2}R_1R_2 + R_1 + R_2)}{[C_1C_2 + C_c(C_1 + C_2)]R_1R_2} \tag{2.19}$$

So the dominant pole of the circuit is

$$f_d = \frac{s_1}{2\pi} = \frac{1}{2\pi R_1[C_1 + C_c(1 + G_{m2}R_2)]} \tag{2.20}$$

Generally, $C_1 \ll C_c$ and $G_{m2}R_2 \gg 1$, so the above equation can be simplified as

$$f_d = \frac{1}{2\pi R_1 R_2 G_{m2} C_c} \tag{2.21}$$

The non-dominant pole is

$$f_{nd} = \frac{s_2}{2\pi} = \frac{G_{m2}C_c}{2\pi(C_1C_2 + C_1C_c + C_2C_c)} \tag{2.22}$$

Since $C_2 \gg C_1$, $C_c \gg C_1$, C_{GS6} dominates C_1, C_L dominates C_2, we can get the GBW approximately.

$$GBW = A_0 f_d = \frac{g_{m1}}{2\pi C_c} \tag{2.23}$$

According to the equation (2.8)

$$GBW = \frac{1}{2\pi C_c}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 V_{GST1} \tag{2.24}$$

Or we can write the formula using current.

$$GBW = \frac{I_{DS1}}{\pi C_c V_{GST1}} \tag{2.25}$$

In the above formula, μ_p and C_{ox} are technological parameters while C_c, W_1, L_1 and V_{GST1} sre design parameters. GBW is directly proportional to channel width and overdrive voltage and is inversely proportional to C_c and L. So we should increase the overdrive voltage or decrease the channel length of MN1 and MN2 to get higher GBW.

However, it is in conflict with increasing the voltage gain and the drop of the area of transistor will make the noise performance worse. So we will trade off the parameters to achieve the performance required.

- **Differential-mode Gain and Common-mode Gain**

If the amplifier is differential-input and single-output, the small signal output voltage can be described as

$$v_0 = A_{dm}V_{id} + A_{cm}v_{ic} \tag{2.26}$$

A_{dm} is the differential-mode gain. $A_{dm} = A_0$ (A_0 is conducted in euqation (2.7)). A_{cm} is the common-mode gain. And the CMRR(Common-mode Rejection Ratio) is defined as

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| \tag{2.27}$$

The CMRR of our circuit is

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| = \left|\frac{v_5}{v_3}\frac{v_3}{v_{id}}\right| / \left|\frac{v_5}{v_3}\frac{v_3}{v_{ic}}\right| = CMRR_1 \tag{2.28}$$

In the above equation, $CMRR_1$ is the CMRR of the first amplification stage. Since the second amplification stage is single-input and single-output, it does not contribute to the global $CMRR$.

According to the feedback gain of the source, the equivalent input transconductance G_m is

$$G_m = \frac{g_{m1}r_{o1}}{2r_{o5} + r_{o1}(1 + g_{m1}2r_{o5})} \tag{2.29}$$

If $g_{m1}r_{o1} \gg 2r_{o5}$, then the expression of G_m can be simplified as

$$G_m \approx \frac{1}{2r_{o5}} \tag{2.30}$$

The output impedance is

$$R_{out} = \frac{1}{g_{m3}}\|r_{o3}\|[2r_{o5} + r_{o1}(1 + g_{m1}r_{o5})] \approx \frac{1}{g_{m3}} \tag{2.31}$$

So the common-mode gain is

$$A_{cm} = G_m R_{out} = \frac{1}{2g_{m3}r_{o5}} \tag{2.32}$$

Substituting the equation (2.7) and (2.32) into equation (2.28), we can get

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| = 2g_{m3}r_{o5}g_{m1}(r_{o2}\|r_{o4}) \tag{2.33}$$

Replace the transconductance with single-output impedance. Ignoring the channel length modulation of the single-output impedance and consdidering $I_{DS1} = I_{DS2} = I_{DS3} = I_{DS4} = I_{DS5}/2$, we can get

$$\begin{aligned} CMRR &= 2\frac{2I_{DS3}}{V_{DSAT3}}\frac{1}{\lambda_P I_{DS5}}\frac{2I_{DS1}}{V_{DSAT1}}\left(\frac{1}{\lambda_P I_{DS2}}\|\frac{1}{\lambda_N I_{DS4}}\right) \\ &= \frac{4}{V_{DSAT1}V_{DSAT3}\lambda_P(\lambda_P + \lambda_N)} \end{aligned} \tag{2.34}$$

We can increase the value of $CMRR$ through decreasing the overdrive voltage. Apart from that, replacing MN5 with high-impedance current source can also improve the $CMRR$, but this method will decrease the common-mode input swing.

- **Slew Rate**

When the input is a large positive step signal, the transistor MN2 will be in cut-off region. The current through MN5 will flow through MN1 and MP3. And the current through MP4 is the same according to the current mirror. Because MN2 is in cut-off region, the current will flow through the C_c. The constant current I_{DS5} flows through

the C_c and produce a voltage gradient, whose slope is $\delta V/\delta t = I_{DS5}/C_c$. If MN7 has enough current to flow to the MP6, the V_{GS6} remains constant and the source voltage of MP4 remains constant, which causes the output voltage increases in gradient. As for the large negative step input, MN1, MP3 and MP4 is cut-off, MN2 works. All the current from MN5 will flow through MN2 and C_c. Given that MN7 has enough current for MP6 to remain the V_{GS6}, the output voltage will have negative gradient with the same slope.
The interior slew rate is

$$SR_{int} = \frac{I_{DS5}}{C_c} \tag{2.35}$$

Later we will connect a load capacitance with the OpAmp to test the slew rate. We set the load capacitance as C_L in the derivation of slew rate.
The load capacitance also needs to store and release charges. Since MP6 is overdrived, releasing charges can be achieved easily. However, C_L stores the charge through MN7, so it must charge in a limited time.
The current through MN7 will flow into C_c and C_L. The current through C_c is I_{DS5}, so the current through C_L is $I_{DS7} - I_{DS5}$. For a positive step input, the source voltage of MP4 and the current through MP6 will decrease. When the C_L is charged by $I_{DS7} - I_{DS5}$, it caused a positive voltage gradient. The slope is

$$SR_{ext} = \frac{I_{DS7} - I_{DS5}}{C_L} \tag{2.36}$$

SR_{ext} is the external slew rate. The critical load capacitance is

$$C_{Lc} = C_c \frac{I_{DS7} - I_{DS5}}{I_{DS5}} \tag{2.37}$$

When C_L is larger than C_Lc, SR is decided by SR_{ext}. Otherwise C_L is decided by SR_{int}. So the overall slew rate SR is the minimum value of the initerior slew rate and the external slew rate.

$$SR = min\left\{\frac{I_{DS5}}{C_c}, \frac{I_{DS7} - I_{DS5}}{C_L}\right\} \tag{2.38}$$

- **Phase Margin**
  To get a phase margin larger than $60°$, the non-dominant point should be larger than 2.2GBW.

$$f_{nd} \geq 2.2GBW \tag{2.39}$$

C. K_n and K_p

1st Method: from model files, K' = μ Cox, Cox= ϵ/tox, where ϵ is the dielectric constant of SiO2. ϵ = ϵox * ϵ0 = 3.9 * 8.854e-14F/cm = 3.46e-11 F/m. Then, from tsmc 0.18/model/spectre/rf018.scs, we can find u0, tox, vth0 of nch and pch. tox(nch) =4e-9m tox(pch) = 4-9m, un = $0.045m^2/v - s$, up = $0.01m^2/v - s$, Vthn=0.2699V, Vthp=0.43V. So **K'n = un * Cox = 0.5 * 0.045 * 3.46e-11 / 4e-9 = 389.2 uA/V**; **K'p = 0.01 * 3.46e-11/4e-9 = 86.5uA/V.**

In our report for the evaluation of the parameters, we use K'p = 50 uA/V; K'n = 100 uA/V for simplification.

2nd Method: we may use Cadence to scan the Idc and detect the voltage to get the μn and μp.

III. Determining the Parameters

To meet the specification, the parameters require elaborately design. The procedure to determine the parameters are as follows. This design procedure assumes that the (differential) gain at dc (Av), the common mode gain at dc (Av), phase margin (PM), unity-gain bandwidth (GBW), load capacitance (CL), slew rate (SR), output voltage swing [Vout(max) and Vout(min)] are given.

- **Minimum Miller capacitor Cc**
  Based on the specifications of Phase Margin $\geq$ 60 degree and Unit Gain Frequency $\geq$ 100 MHz. For the desired two stage phase margin $\geq$ 60 degree, the Miller capacitor should be:

$$Cc \geq 0.22CL(WillySansen) \tag{3.1}$$

  Considering the pole and stability in the Follow-up requirements, in this design, we choose Cc = 0.26 pF.
- **Minimum "Tail Current" (I_{dc5})**
  Given the slew rate requirement, we can calculate the I_{dc5} from the largest of the two value:

$$I_{dc5} = SR \cdot C_c \tag{3.2}$$

  This equation gives $I_{dc5} \geq 2.6\mu A$. However, to make sure the Gain Bandwidth, we use current mirror to offer 30 μA.
- **Value of $g_{m1,2}$**
  Since

$$GBW = \frac{g_{m1,2}}{2\pi C_c} \tag{3.3}$$

  so we have

$$g_{m1,2} = GBW \cdot 2\pi C_c \tag{3.4}$$

  Thus the value is gm1,2 = 100 MHz $\times$ 0.26 pF $\times$ = 163.362 μS.
- **Value of gm6**
  We know that

$$f2 = \frac{g_{m6}}{2\pi \cdot C_L} \tag{3.5}$$

  And to implement the phase margin of 60 degree, the relationship between dominant pole and first non-dominant pole is f2 = 2.2 f1. So we get value of gm6 :

$$g_{m6} = 2.2 g_{m1,2} \frac{C_L}{C_c} \tag{3.6}$$

  Therefore, gm6 = 1382.293 μS.
- **Miller Compensation Rc**
  We have already calculated the zero point in the upper part:

$$f_Z = \frac{1}{2\pi C_c(1/g_{m6} - R_c)} \tag{3.7}$$

  We don't want the right half plane zero, which will increase the gain but decrease phase margin, which will

cause the instability. If Rc $\gg$ 1/gm6, zero $\approx -\frac{1}{2\pi C_c R_c}$. To meet the phase margin requirement, we need $f_z > f_nd$ and $f_{nd} = 2.2GBW$. So we get:

$$\frac{1}{g_{m6}} < R_c < \frac{1}{2.2g_{m1,2}} \tag{3.8}$$

Rc is used for the negative zero compensation. Given the previous 2 steps, we get range of Rc is $723.436\Omega < R_c < 2782.443\Omega$. In this design, we finally choose 1320.92 Ω.

- Determining $(\frac{W}{L})_{1,2}$

Since we have figured out the value of gm1,2, now we can determine the aspect ratio (size) of MOS MN1 and MN2. Given equation of gm:

$$g_{m1,2} = \sqrt{2\mu C_{ox}(\frac{W}{L})_{1,2} I_{dc1,2}} \tag{3.9}$$

$$I_{dc1,2} = 1/2 \cdot I_{dc5} \tag{3.10}$$

Thus, we get

$$(\frac{W}{L})_{1,2} = \frac{g_{m1,2}^2}{\mu n C_{ox} I_{dc5}} \approx 10.767 \tag{3.11}$$

Since this is only a value of evaluation, there might be some errors. Actually in our design, after considering the Gain and GBW, the aspect ratio in our design of MOS MN1 and MN2 is

$$(\frac{W}{L})_{1,2} = \frac{5.68\mu m}{400nm} = 14.2 \tag{3.12}$$

- **Value of** $(\frac{W}{L})_{3,4}$

The aspect ratio of MOS MP3, MP4 has to satisfy a relationship:

$$(\frac{W}{L})_{3,4} = \frac{I_{dc5}}{(K_3')[V_{DD} - V_{in}(max) - |V_{T0}|(max) + V_{T1}(min)]^2} \tag{3.13}$$

After look up some value of the model, we get that

$$(\frac{W}{L})_{3,4} \approx 45 \tag{3.14}$$

Similarly, this is not an exact value. Considering other factors, we adjust the ratio to

$$(\frac{W}{L})_{3,4} = \frac{12.213\mu m}{190nm} \approx 64 \tag{3.15}$$

- **Value of gm3,4**

Similar as calculation of gm1,2, we apply the formula of gm to get:

$$g_{m3,4} = \sqrt{2I_{dc3,4}K'p(\frac{W}{L})_{3,4}} \tag{3.16}$$

where assume K'p = 50×10^{-6}, we get gm3,4 $\approx$ 259.8 μS.

- **Value of** $(\frac{W}{L})_6$

Given the relationship:

$$(\frac{W}{L})_6 = (\frac{W}{L})_{3,4}\frac{g_{m6}}{g_{m3,4}} \tag{3.17}$$

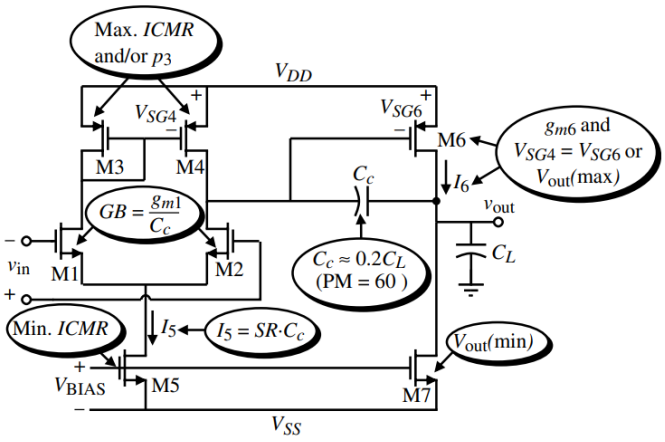

Fig. 4. Illustration of the Design Relationship and the Circuit for a Two Stage CMOS Op Amp

we get that

$$(\frac{W}{L})_6 = 45 \times \frac{1382.293}{259.6} \approx 239 \tag{3.18}$$

Then we set aspect ratio to

$$(\frac{W}{L})_6 = \frac{73.266\mu m}{190nm} \approx 385 \tag{3.19}$$

- **Determine** I_{dc6}

Given the value of $(\frac{W}{L})_6$, g,6, K'p, we may evaluate the value of I_{dc6}:

$$I_{dc6} = \frac{g_{m6}^2}{2K'p(\frac{W}{L})_6} \tag{3.20}$$

$$I_{dc6} = \frac{1382.293^2}{2 \times 50 \times 10(-6) \times 239} \approx 79.68\mu m \tag{3.21}$$

In our design, we set $I_{dc6} \approx 90uA$.

- **Aspect Ratio for Current Mirror**

The MOS for current mirror are MN5, MN7, MN8. According the analysis above, we might design the current through each MOS are 30 uA, 90 uA and 5 uA (as the bias). Thus the aspect ration should satisfy:

$$(\frac{W}{L})_5 : (\frac{W}{L})_7 : (\frac{W}{L})_8 = 6 : 18 : 1 \tag{3.22}$$

In this circuit design, we set

$$(\frac{W}{L})_5 : (\frac{W}{L})_7 : (\frac{W}{L})_8 = \frac{12um}{2um} : \frac{36um}{2um} : \frac{2um}{2um} \tag{3.23}$$

IV. Overall Analysis and Optimism

The overall illustration of the design relationship and the circuit for a two stage CMOS op amp is shown in fig 4

The fig 5 shows the dependence of the Performance on dc Current, W/L Ratios and the Compensating. It is not enough to determine the parameter to meet the requirement just by theoretically calculation. To consider all the factors, we need to be clear about some relationships shown in fig 5.

	Drain Current		M1 and M2		M3 and M4		Inverter	Inverter Load		Compensation Capacitor
	I_5	I_7	W/L	L	W	L	W_6/L_6	W_7	L_7	C_c
Increase dc Gain	$(\downarrow)^{1/2}$	$(\downarrow)^{1/2}$	$(\uparrow)^{1/2}$	$\uparrow$		$\uparrow$	$(\uparrow)^{1/2}$		$\uparrow$	
Increase GB	$(\uparrow)^{1/2}$		$(\uparrow)^{1/2}$							$\downarrow$
Increase RHP Zero		$(\uparrow)^{1/2}$					$(\uparrow)^{1/2}$			$\downarrow$
Increase Slew Rate	$\uparrow$									$\downarrow$
Increase C_L										$\uparrow$

Fig. 5. Dependence of the Performance on dc Current, W/L Ratios and the Compensating.

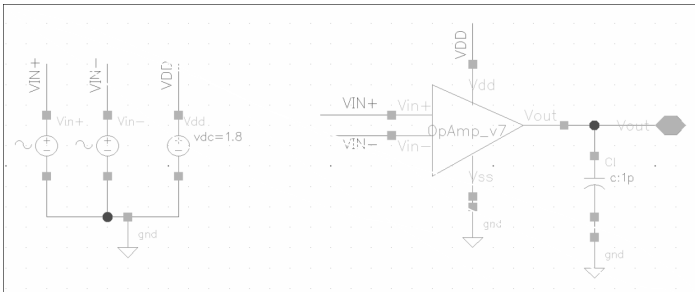

Fig. 6. Test Bench for Open-Loop Differential-Mode Gain and Common-Mode Gain Simulation.

V. Simulation Results

Below will show the simulations of some specifications for a Typical Unbuffered CMOS Op Amp in this experiment. Each Simulation contains test bench, ADE L settings, simulation results and analysis.

A. A_{DM0} Open-Loop Differential-Mode Gain Simulation

The test bench is shown in fig 6. The Vdd = 1.8 V (as required). Set Vcm = 900 mV (this is because the input range to satisfy MOS M3, M4, and current mirror MOS M8, M5 all work in the saturation region). The AC magnitude = 500 mV (if we do so, the A_{DM0} simulation will be simplified by only plot the V_{out} in 20 dB mode). The phase of V_{in+} and V_{in-} are 0 and 180 degree, respectively.

The plot in fig 7 shows A_{DM0} = 61.9899 dB, which shows $A_{DM0} \geq 1000V/V$, which meets the requirements.

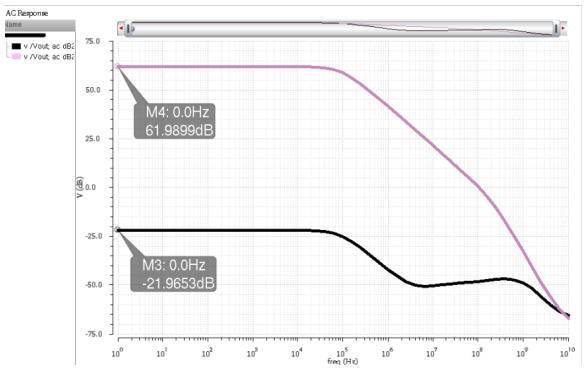

Fig. 7. Simulation results of A_{DM0} and A_{CM0} in 20 dB form.

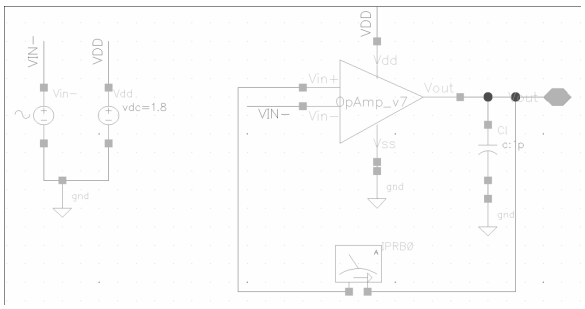

Fig. 8. Test Bench for Phase Margin and Unit Gain Frequency Simulation.

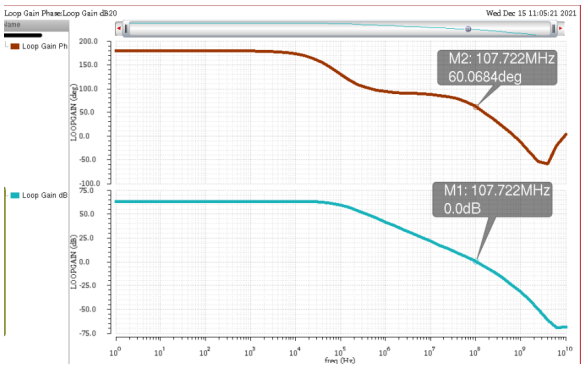

Fig. 9. Simulation results of Phase Margin and Unit Gain Frequency.

B. A_{CM0} Open-Loop Common-Mode Gain Simulation

The test bench similar with fig 6. The Vdd, Vcm, magnitude of V_{in+} and V_{in-} are the same as Different-Mode. But the phase of V_{in+} and V_{in-} are 0 the same.

The plot in fig 7 shows A_{DM0} = -21.9653 dB, which shows $A_{DM0} \leq 0.1V/V$, which also meets the requirements.

Actually, there are another way to discribe, Common-mode rejection ratio (CMRR).

$$CMRR = \frac{A_{DM0}}{A_{CM0}} \tag{5.1}$$

(If need), we can get CMRR of this OpAmp eauqls 83.9552 dB, $\geq 60dB$. The greater this is, say the larger gap bewteen A_{DM0} and A_{CM0}, the higher gain the amplifier is.

C. Phase Margin

The Phase Margin test bench should in closed-loop as shown in fig 8.

The Phase Margin of this design is 60.0684 degree, $\geq$ 60degree as required (fig 9).

D. Unit Gain Frequency

The Unit Gain Frequency test bench should also in closed-loop as shown in fig 8.

The Unit Gain Frequency of this design is 107.722MHz, $\geq$ 100MHz as required (fig 9).

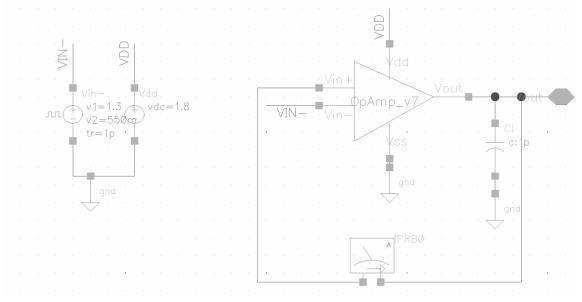

Fig. 10. Test Bench for Slew Rate.

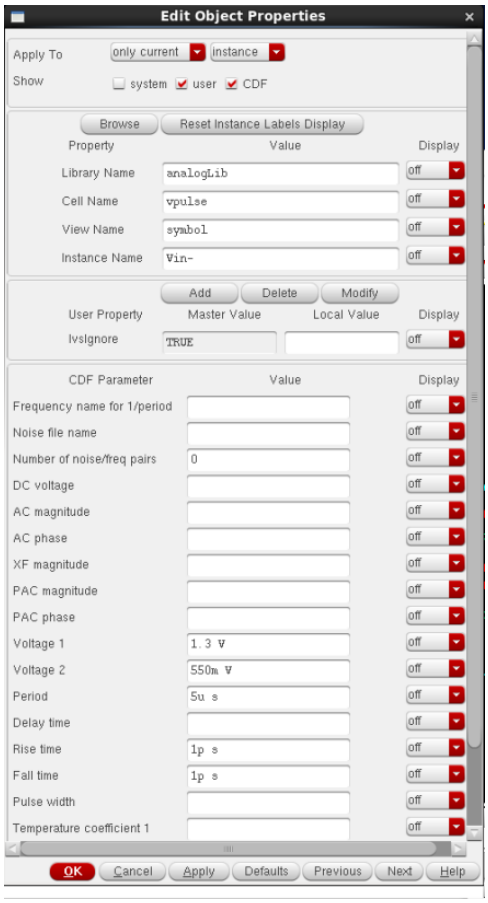

Fig. 11. vpulse settings for test bench of slew rate.

E. Slew Rate

The Slew Rate test bench is shown in fig 10. In this test bench, we use the vpluse rather than vsin in Vin- port. In vpluse, the v_{max} = 1.3V, v_{min} = 550mV, rise time 1 ps, fall time = 1ps and period = 5 us (fig 11).

Now calculate the slew rate at rise edge and fall edge.

Firstly, the rise edge: in fig 13, we find that $slewrate_{rise}$ = 120.67 MV/s = 120.67 V/us.

As for the rise edge: in fig 14, we find that $slewrate_{fall}$ = 57.9608 MV/s = 57.9608 V/us.

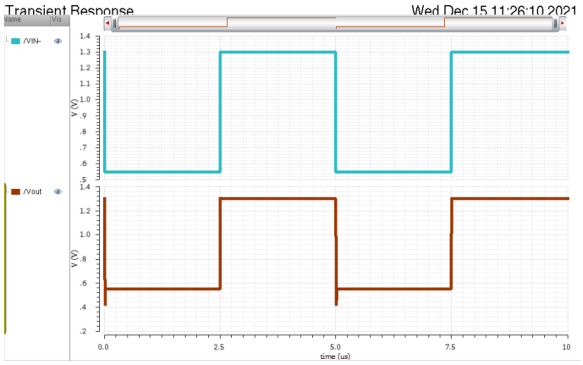

Fig. 12. Plot for Slew Rate, overall view.

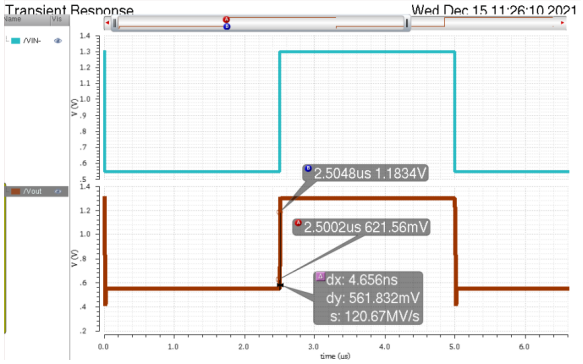

Fig. 13. Plot for Slew Rate, rise edge.

Both $slewrate_{rise}$ and $slewrate_{fall}$ meet the specifications which is "slew rate $\geq$ 10 V/us".

F. Output Swing

The test bench to get the output swing is shown in fig 15. This time we use "vsin" again, but the properties are different: for big signal properties, we set amplitude = 500mV, initial phase = 0, frequency = 800 kHz (fig 16).

We can calculate the output swing in fig 17: swing $\geq$ 1.387-0.412V = 0.975 V . To get the maximum value of Vmax-Vmin without the distortion, we scan the amplitude of vsin

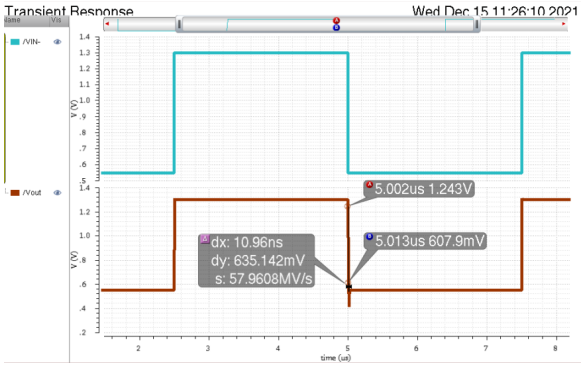

Fig. 14. Plot for Slew Rate, fall edge.

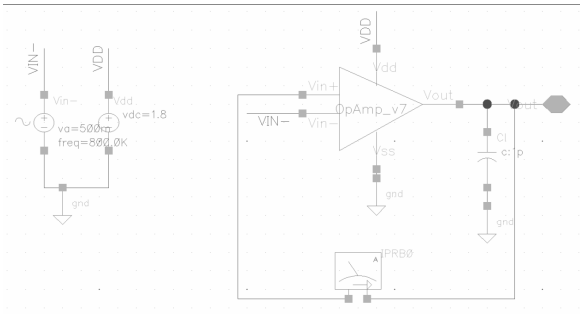

Fig. 15. Test Bench for output swing

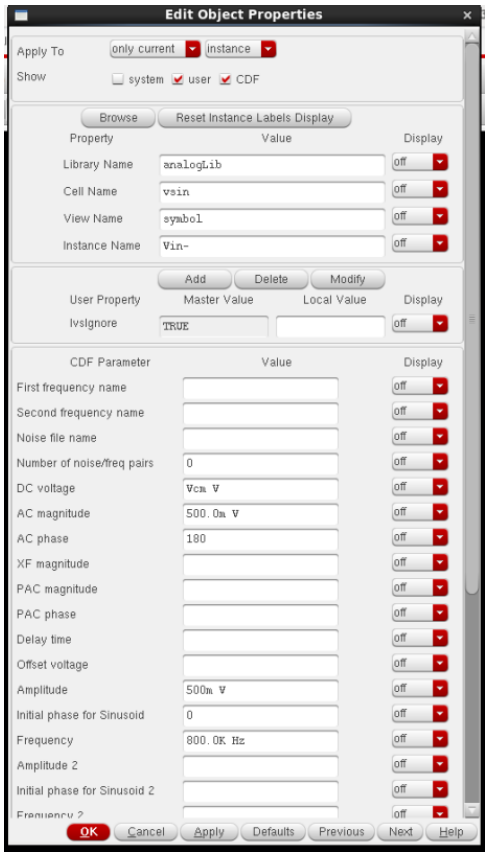

Fig. 16. vsin settings in test bench of output swing.

(fig 18). The noted two points in fig **??** give the output swing is about 1.50344 V - 312.084 mV = 1.191356 V. Obviously, this satisfies the requirement $\geq$ 800 mV.

G. Power Consumption

From fig. 19, we get the exact current of each branch, then we can calculate the power consumption:

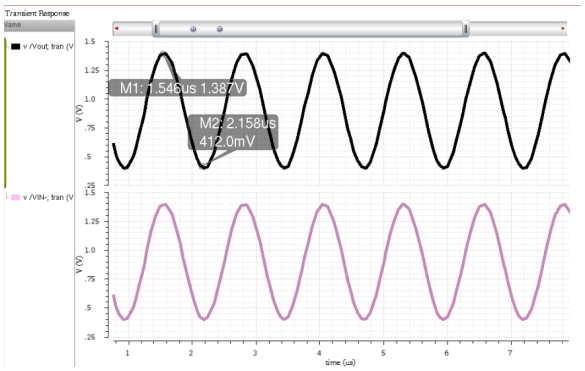

Fig. 17. Plot for output swing, which shows output swing will be greater than 900mV

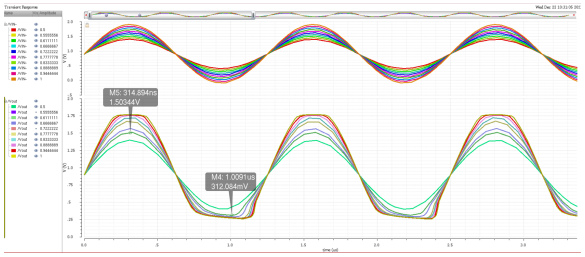

Fig. 18. Scan the amplitude of vin- from 500 mV to 1 V, we can get the max value of Vmax-Vmin, or say, output swing.

TABLE I
TRANSISTOR PARAMETERS

Transistor	Aspect Ratio W/L	Theoretical Current
MN1	5.66μm/400nm	15 μ A
MN2	5.66μm/400nm	15 μ A
MP3	12.213μm/190nm	15 μ A
MP4	12.213μm/190nm	15 μ A
MN5	12μm/2μm	30 μ A
MP6	73.266μm/190nm	90 μ A
MN7	36μm/2μm	90 μ A
MN8	2μm/2μm	5 μ A

TABLE II
ELEMENTS FOR MILLER COMPENSATION

Element	Parameter
R_c	1320.92 Ω
C_c	0.26 pF

TABLE III
CIRCUIT PERFORMANCE

Parameter	Requirement	Proposed Design
A_{DM0}	$\geq$ 1000 V/V	1257.5 V/V
A_{CM0}	$\leq$ 0.1 V/V	0.07975 V/V
Phase Margin	$\geq$ 60°	60.0684°
Unit Gain Frequency	$\geq$ 100 MHz	107.722 MHz
Slew Rate	$\geq 10V/\mu s$	120.67 V/μs @ rise edge 57.96 V/μs @ fall edge
Output Voltage Swing	$\geq$ 800 mVpp	1191.356 mV
Power	minimum	232.25616 μW

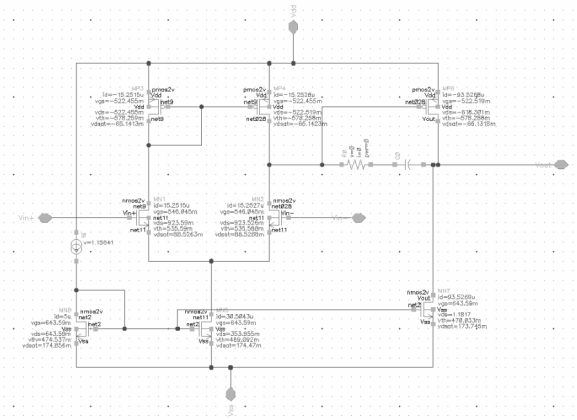

Fig. 19. Circuit noted with the DC operating point

P = $I_{total} \times Vdd$

= ($I_{MN8} + I_{MN5} + I_{MN7}$) $\times Vdd$

= (5u + 30.5043u + 93.5269u) $\times 1.8V$

= 232.25616 μW (5.2)

This equation gives the power consumption of our design is 232.25616 μW.

VI. Conclusion

A. Parameters of Circuit Elements

In conclusion, the aspect ratio of 8 MOS are shown in table I. The design methods are based on all the analysis mentioned above. Note that all the evaluations are for reference only, and the simulation results are another significant part for the adjustment of parameters, as the trend is shown in fig 5. In our design, to deal with the stability, we add the Miller resistance R_c and Miller capacitance C_c. The derivation of R_c and C_c is shown in "Determining the Parameters" part, specifically, their values are shown in table II.

B. Performance

Table III gives the comparison of performance of our design and the requirements. The performance of our design can satisfy the specifications as well as a low power consumption. In conclusion, this report demonstrate a two-stage high gain low power Op Amp.

Acknowledgment

We would like to acknowledge Professor, Quan Pan, for inspiring our interest in the design of integrated circuit and Op Amp. Our teaching assistants also help a lot.For this, we are extremely grateful.

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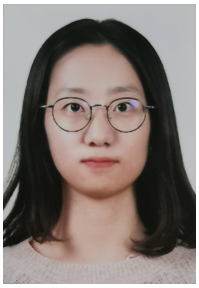
Shuo Feng Shuo Feng is a year-2019 undergraduate student. She is involved in the study and research of ICs design with Prof. Quan Pan's group.

Office: 18306665189

Email: 11911736@mail.sustech.edu.cn



Haoyu Wang Haoyu Wang is a year-2019 undergraduate student. She is involved in the study and research of deep learning IC design with Prof. Hao Yu's group.

Office: 13997690736

Email: 11911134@mail.sustech.edu.cn