# A 4-$V_{ppd}$ 160-Gb/s PAM-4 Optical Modulator Driver with All-Pass Filter-Based Dynamic Bias and 2-Tap FFE in 130-nm BiCMOS

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***Abstract*—This paper presents a high-speed, large-output swing driver with 2-tap feed-forward equalizer (FFE) for optical modulators in 130-nm SiGe BiCMOS process. A breakdown voltage (BV) doubler topology with all-pass filter (APF)-based dynamic bias is applied in the driver to improve the output swing and the bandwidth. A 2-tap fractional-spaced FFE is implemented to compensate for the insufficient bandwidth of optical modulators. Simulation results indicate that the driver achieves an output swing of 4 $V_{ppd}$ and a 3-dB bandwidth of 62.4 GHz with a power consumption of 1.15 W. The performance of the driver is further evaluated in an electrical/optical (E/O) system where a Verilog-A model for Mach-Zehnder Modulator (MZM) with a 3-dB bandwidth of 35 GHz is used. Taking advantages of the 2-tap FFE, the E/O system achieves a 3-dB bandwidth of 50.4 GHz and can support 160-Gb/s PAM-4 optical communications.**

***Keywords—all-pass filter, breakdown voltage doubler, electrical-optical system, feed-forward equalizer, optical modulator driver***

## I. Introduction

With the rapid development of internet of things (IoT), artificial intelligence (AI) and cloud computing, high-performance optical communication systems are of significance in data centers and metro networks for improving communication capacities. In order to improve the speed and the extinction ratio (ER) of optical signals generated by optical modulators, a driver with high bandwidth and large output voltage swing is essential. However, the signal degradation due to the frequency-dependent loss of optical modulators makes stringent demands on the equalization techniques at the driver side.

In previous works, there are mainly two approaches to achieving large-swing drivers. The first utilizes distributed amplifier topologies with multiple cascading stages, such as [1], which results in high-circuitry complexity and low bandwidth. The other method is using a breakdown voltage (BV) doubler structure with dynamic bias circuit to avoid the breakdown of the cascode transistor and thus to improve the output voltage swing [2]. Based on [2], [3] uses an additional emitter follower (EF) stage and applies negative miller capacitance (NMC) to enhance the bandwidth. Further, [4] combines the BV doubler with a resistor-based capacitor-splitting topology to increase the bandwidth. However, the dynamic bias circuits applied in [2]-[4] are all based on the low-pass filter (LPF) structure, where the shape and the phase of the generated bias signal for the base of cascode transistor will be distorted with the increase of the input signal rate. The issue will degrade the bandwidth performance of the cascode transistor and the whole driver. To overcome the problem, this work proposes a BV doubler topology with all-pass filter (APF)-based bias circuit to relieve the distortion of the bias signal and to enhance the bandwidth of the driver.

In addition, although multiple large-swing drivers for optical modulators are proposed recently, few of them have concerned the equalization needs of optical modulators whose bandwidth is typically the limitation of the electrical/optical (E/O) systems. In this work, we analyze and compare the merits and drawbacks of widely used equalization techniques including continuous-time linear equalizer (CTLE), decision-feedback equalizer (DFE) and feed-forward equalizer (FFE) [5]-[7], and incorporate a re-configurable 2-tap fractional-spaced FFE implemented at the data path before the large-swing driver core. To ensure the FFE can be more applicable for optical modulators, an E/O system with a Verilog-A model for Mach-Zehnder Modulator (MZM) of 35-GHz 3-dB bandwidth is built to enable the E/O co-design and co-simulation.

The remain of this paper is organized as follows. Section II illustrates the circuit implementation of the proposed driver, from the general architecture to the detailed circuits of each stage. Section III demonstrates the performance of the proposed driver by presenting the simulation results. Therewith, a comparison with state of the arts is provided. Finally, Section IV draws the conclusion.

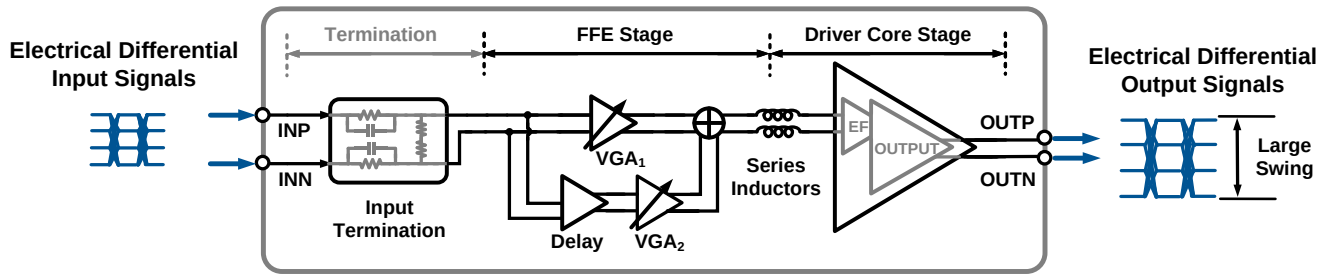

Fig. 1. Block diagram of the proposed optical modulator driver.

## II. Circuit Implementation

### A. Architecture of the Driver

The block diagram of the proposed optical modulator driver is shown in Fig. 1, mainly including an FFE stage and a driver core stage. After comparing the characteristics of various equalizers, FFE is chosen for equalization stage. The key part of the large-swing driver core is the output stage, which determines the achievable output voltage swing and the bandwidth of the driver. This is also one of the main contributions of this work. Series inductors are inserted between the two stages to cancel out the parasitic capacitance of the inter-mediate nodes. Besides, an input termination with a passive equalizer is implemented at the input port to improve the bandwidth and the input reflection performance of the driver.

### B. FFE Stage

Equalization techniques are widely used in high-speed circuit designs to compensate the low-pass characteristics of communication devices and channels. The mainstream equalizers include CTLE, DFE and FFE [5]-[7]. CTLE

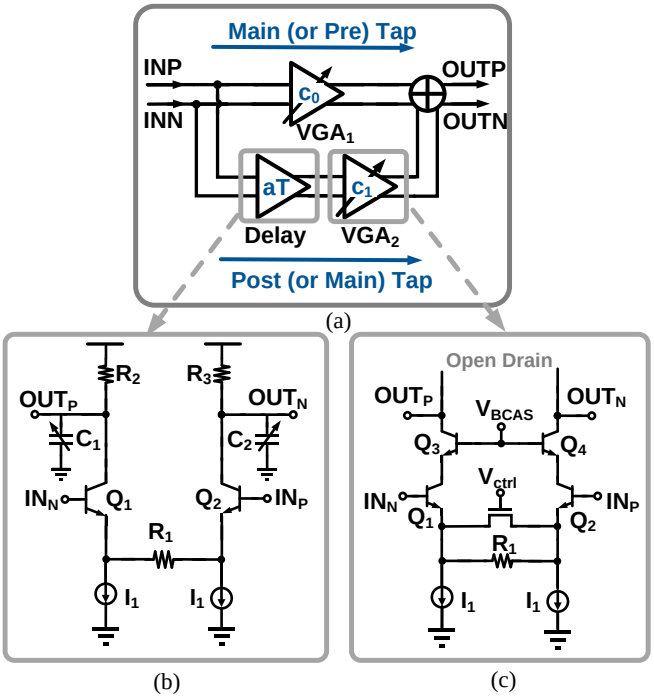


Fig. 2. (a) Block diagram of 2-tap fractional-spaced feed-forward equalizer (FFE). (b) Schematic of the delay cell. (c) Schematic of the variable-gain amplifiers (VGAs).

implemented by proper arrangement of the poles and zeros has two main drawbacks: the relatively fixed rising slope of 20 dB/decade and the unavoidable noise amplification [5], [6]. The nonlinear equalizer DFE, with the algorithm of reducing inter-symbol interference (ISI) based on the detected data, has insufficient time margin for high-speed signals [5], [7]. Another equalization method, FFE, has a structure identical to a finite impulse response (FIR) filter, with the signal passing through delayed elements and each delayed signal being multiplied by a coefficient of a different weight. Considering the unwanted noise amplification and fixed peaking slope of CTLE, as well as the insignificant high-frequency compensation capacity of DFE, FFE provides greater equalization flexibility without the noise magnification [5].

In this work, a re-configurable FFE is proposed to extend the limited bandwidth of the optical modulators. The proposed FFE can support the mode of one pre-tap and one main-tap, as well as the mode of one main-tap and one post-tap. The re-configurable property ensures that the proposed FFE can be adapted to various optical modulators with different frequency characteristics. The block diagram of the proposed FFE is shown in Fig. 2(a).

A delay cell is inserted in the post (or main)-tap path to generate the delayed signal for equalization. The schematic of the delay cell is shown in Fig. 2(b). Capacitors C1-C2 are applied to introduce a pole for delay control. The delay cell provides an adjustable delay of less than 1 UI, resulting in a fractional-spaced FFE that enables the bandwidth compensation beyond the Nyquist frequency.

Variable-gain amplifiers (VGAs) are implemented in both paths, as shown in Fig. 2(c). The cascode transistors Q3-Q4 provide an isolation between the input and output nodes. Besides, the VGAs are designed in an open-drain style so that the signals from the two paths can be added at the output nodes in the form of current. The switch of the two FFE modes is achieved by controlling the gain and polarity of the VGAs.

### C. Driver Core Stage

The schematic of the proposed driver core stage is shown in Fig. 3, consisting of an emitter follower (EF) stage and an OUTPUT stage with APF-based dynamic bias circuit. The EF stage (transistors $Q_1$-$Q_2$) acts as a buffer to isolate the previous FFE stage and the OUTPUT stage, as well as to shift down the DC common-mode level of the input signals.

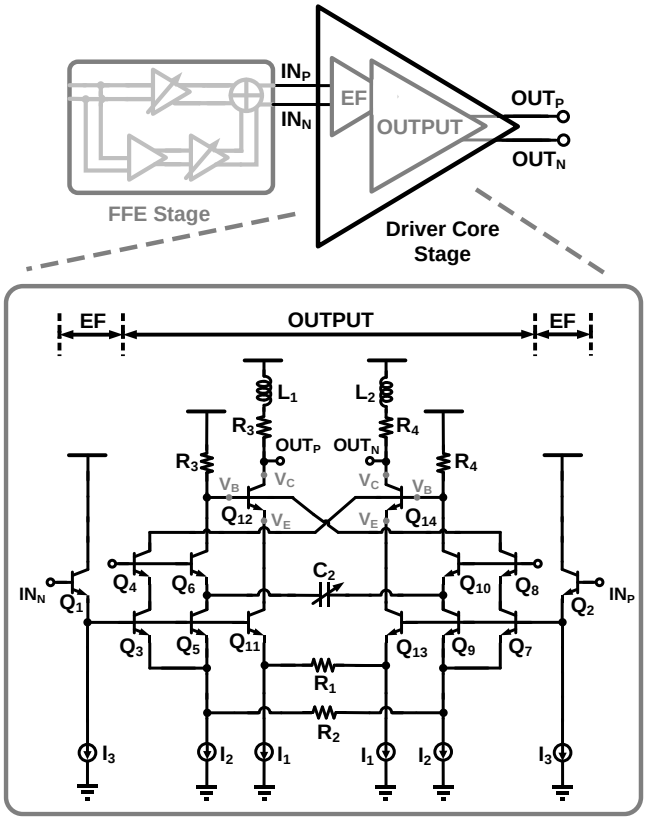

Fig. 3. Schematic of the proposed BV doubler topology driver core with all-pass filter (APF)-based bias.

Limited by small collector-emitter breakdown voltage ($BV_{CEO}$) of SiGe hetero-junction bipolar transistor (HBT), a traditional cascode-based driver with the base of each cascode transistor biased at a fixed voltage can only achieve an output voltage swing smaller than $BV_{CEO}$. To relieve the issue, a BV doubler topology is adopted in the output stage of this diver core, as shown in Fig. 3. Since the emitter voltage $V_E$, the base voltage $V_B$ and the collector voltage $V_C$ of transistor $Q_{12}$ (or transistor $Q_{14}$) in Fig. 3 are in phase, and $V_E$ varies with $V_B$, the output voltage swing of the output stage can be twice that of the conventional cascode-based driver by properly controlling the swing and the phase of $V_B$.

To generate $V_B$, prior works [2]-[4] use the low-pass filter (LPF)-based dynamic bias circuits as illustrated in Fig. 4, with a transfer function shown as follows:

$$H(j\omega) = \frac{G}{1 + j\omega\tau} \qquad (1)$$

where 'G' represents a gain of LPF, and '$1/\tau$' is a LPF pole. However, to optimize the group delay performance of the driver, loading varactors $C_1$-$C_2$ as shown in Fig. 4 are typically inserted at the output nodes of the bias circuit to tune '$\tau$' in (1). The larger '$\tau$' is, the lower bandwidth of the bias circuit, resulting in the distortion of the generated bias signals when the driver is operating at a high speed.

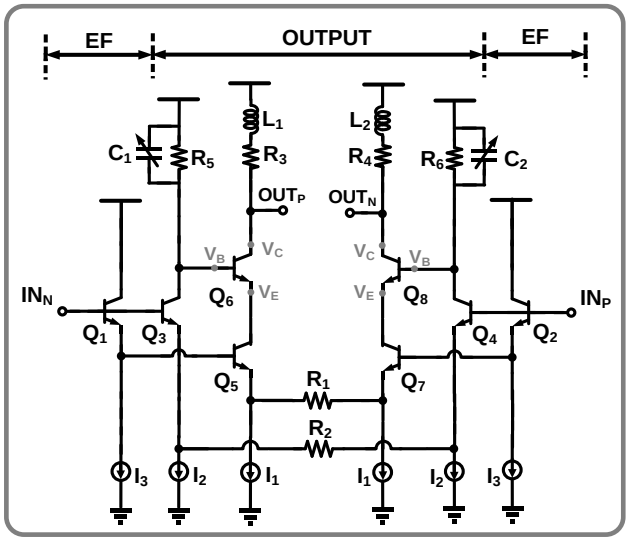


Fig. 4. Schematic of the conventional BV doubler topology driver with low-pass filter (LPF)-based bias.

In this work, an APF-based dynamic bias circuit (transistors $Q_3$-$Q_{10}$), as shown in Fig. 3, is proposed to relieve the above distortion issue in the output stage. The transfer function of APF can be estimated as [8]:

$$H(j\omega) = G \cdot \frac{1 - j\omega\tau}{1 + j\omega\tau} = G \cdot \left(\frac{2}{1 + j\omega\tau} - 1\right) \qquad (2)$$

again, 'G' represents a gain of APF, and there is a zero and a pole overlapping at the same frequency '$1/\tau$'. The deformation of (2) suggests that the APF-based bias circuit can be obtained by the combination of a single-pole LPF ($Q_5$, $Q_6$, $Q_9$, $Q_{10}$) with a normalized gain of '2' and an inverted APF ($Q_3$, $Q_4$, $Q_7$, $Q_8$) with a normalized gain of '$-1$', as shown in Fig. 3. A varactor $C_2$ is introduced to tune the delay of the bias circuit by controlling the '$\tau$'. As can be seen from (2), the variation of '$\tau$' does not affect the bandwidth of the filter due to the zero-pole-overlapping, so that the relationship between the bandwidth and the delay of the bias circuit can be decoupled. Since loading varactors are no longer needed, the bandwidth of the bias circuit can be significantly improved.

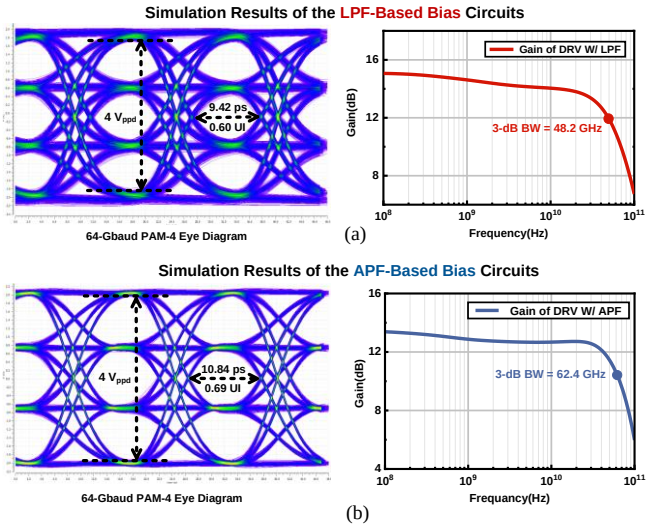


Fig. 5. (a) 64-Gbaud PAM-4 eye diagram (left) and the frequency response (right) of the driver with LPF-based bias circuit. (b) 64-Gbaud PAM-4 eye diagram (left) and the frequency response (right) of the driver with APF-based bias circuit.

Simulations are performed to verify the superiority of the proposed APF-based bias circuit. Fig. 5(a) shows the simulation results of the driver with LPF-based bias circuit. Fig. 5(b) shows the simulation results of the driver with APF-based bias circuit. With the close power consumption and the same output swing of 4 $V_{ppd}$, the APF-based version achieves a 29% extension in bandwidth, from 48.2 GHz to 62.4 GHz, compared with the LPF-based version, and increases the ratio of level mismatch (RLM) from 91.2% to 95.1% for the 64-Gbaud PAM-4 signal. Moreover, the simulated eye width is improved from 0.60 UI to 0.69 UI.

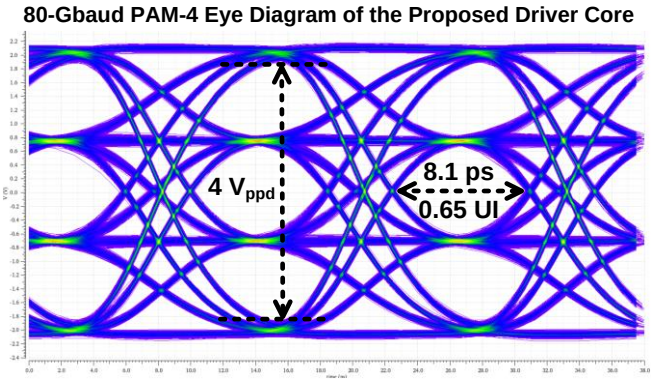


Fig. 6. 80-Gbaud PAM-4 eye diagram of the proposed driver.

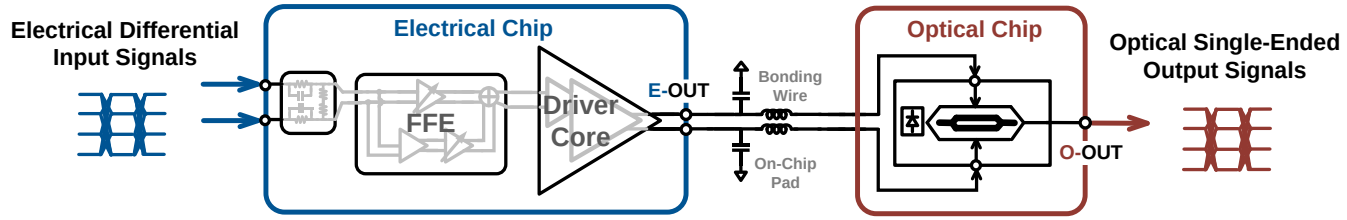


Fig. 7. Electrical/optical (E/O) system with the proposed electrical driver and the optical MZM modulator.

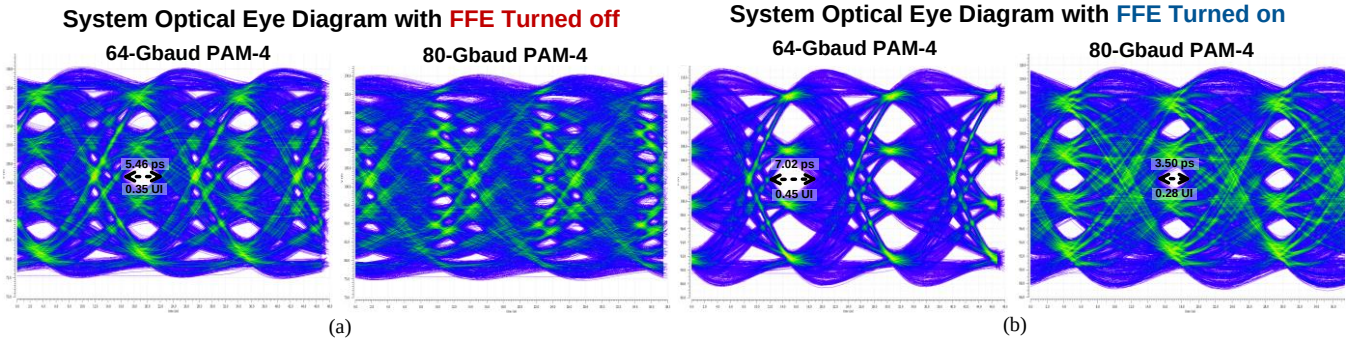


Fig. 8. (a) 64-Gbaud PAM-4 (left) and 80-Gbaud PAM-4 (right) E/O system optical eye diagram with FFE turned off. (b) 64-Gbaud PAM-4 (left) and 80-Gbaud PAM-4 (right) E/O system optical eye diagram with FFE turned on.

The performance of the proposed driver is further simulated using input signals of a higher speed, as shown in Fig. 6. Simulation results demonstrate a clear-opened 80-Gbaud PAM-4 eye diagram with a 4-$V_{ppd}$ output voltage swing and a 0.65-UI eye width. And the RLM is 94.7%. The simulation results indicate that the driver achieves a large output swing, a sufficiently high bandwidth, as well as a good linearity.

## III. E/O System Simulation Results

To fully evaluate the performance of the proposed driver, as shown in Fig. 7, an E/O system is built for co-simulation, where a Verilog-A model for MZM with a 3-dB bandwidth of 35 GHz is used. The impacts of on-chip pads and bonding wires are also considered.

Fig. 8(a) shows the E/O system optical output eye diagrams of 64-Gbaud PAM-4 (left) and 80-Gbaud PAM-4 (right) when FFE is turned off. Without FFE, the width of the eye diagram for 64-Gbaud PAM-4 is 0.35 UI and the RLM is 90.1%, while the eye diagram for 80-Gbaud PAM-4 is completely closed. Fig. 8(b) shows the E/O system optical output eye diagrams of 64-Gbaud PAM-4 (left) and 80-Gbaud PAM-4 (right) when FFE is turned on. Compared with the results of the case when FFE is turned off, the 64-Gbaud PAM-4 eye diagram has a larger eye height with a RLM of 93.1%, and a wider eye width of 0.45 UI. The eye diagram for 80-Gbaud PAM-4 is still opened with a 0.28-UI eye width and a 91.3% RLM. Moreover, the frequency response of the E/O system when FFE is turned off and turned on is shown in Fig. 9, which illustrates a 74% enhancement of the 3-dB bandwidth from 28.9 GHz to 50.4 GHz.

Table I summarizes the performance of the proposed driver and a comparison with state of the arts. Compared with [4] which uses the same technology node, the proposed driver achieves a higher simulated output swing of PAM-4 signals at a close power consumption. Compared with [10] and [11], which utilize more advanced technology node, the proposed driver supports PAM-4 amplifications with higher data rates. When compared with [12], the output swing of our work can reach about 2.7 times of it. In [12], a four-channel transmitter with similar date rate per channel as our work, the most remarkable feature is that the power consumption of a single optical modulator driver is lower, leading us to plan the implementation of this idea in 55-nm CMOS for further comparison in the next step.

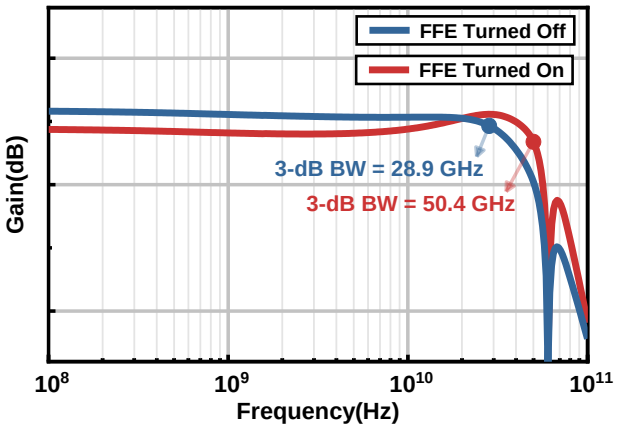


Fig. 9. Simulated frequency response of the E/O system with FFE turned off and turned on.

TABLE I. Comparison Tabel with State of the Arts

| | [4] | [9] | [10] | [11] | [12] | This Work[a] |
|---|---|---|---|---|---|---|
| **Technology** | 130-nm SiGe BiCMOS | 250-nm InP DHBT | 55-nm SiGe BiCMOS | 55-nm SiGe BiCMOS | 65-nm CMOS | 130-nm SiGe BiCMOS |
| **Differential Output Swing (V)** | 2.4 @PAM-4 | 1.8 @PAM-4 | 4.8 @PAM-4 | 4.4 @PAM-4 | 1.5 @PAM-4 | 4 @PAM-4 |
| **Electrical BW (GHz)** | > 40 | 67 | 57.5 | > 70 | 48 | 62 |
| **E/O BW (GHz)** | 40 | N.A. | N.A. | N.A. | 43 | 50.4 |
| **Data Rate (Gb/s)** | 552 @ DP-16QAM | 112 @ PAM-4 | 128 @ PAM-4 | 128 @ PAM-4 | 640 @ DP-32QAM | 160 @ PAM-4 |
| **Gain @ 1 GHz** | 20-30 | 1-11 | 12.8 | 20 | 13-22.5 | 13.4 |
| **Power (W)** | 4 | 0.84 | 0.82 | 1.1 | 0.9 | 1.15 (driver core: 0.99) |

[a] simulated results.

## IV. Conclusion

A 160-Gb/s PAM-4 optical modulator driver with APF-based dynamic bias circuit and 2-tap FFE in 130-nm SiGe BiCMOS process is proposed in this work. The effectiveness of the proposed APF-based dynamic bias circuit is strongly confirmed by theoretical analysis and simulations. With the aid of the APF-based bias circuit, the driver achieves a 3-dB bandwidth of 62.4 GHz and an output voltage swing of 4 $V_{ppd}$.

The performance of the proposed driver is further verified in an E/O system. E/O simulation results demonstrate that the proposed 2-tap FFE can enhance the E/O bandwidth by 74% from 28.9 GHz to 50.4 GHz using an MZM Model with a 3-dB bandwidth of 35 GHz. The E/O system can clearly open an 80-Gbaud PAM-4 optical eye with a width of 0.28 UI and a RLM of 91.3%, indicating that the proposed driver can support the PAM-4 optical communications with a data rate as high as 160 Gb/s.

## Acknowledgment

This work was supported in part by STPSZ under Grants JCYJ20190809142017428 and JCYJ20200109141225025, and in part by NSFC under Grant 62074074, in part by NSFGP under Grant 2021A1515011266 and in part by NSQKJJ under Grant K21799121.

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